IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) ~~The~~An insulated gate field effect transistor ~~according to claim 1~~having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity type source area thereof, wherein:

said channel area provides a single channel between said first and second conductivity type source areas and includes a non-overlapped area portion free from being overlapped by the gate electrode in plan, wherein:

said channel area is comprised of a polycrystal silicon film.

3. (Previously Presented) The field effect transistor according to claim 2, wherein:

the non-overlapped area portion of said channel area has a length longer than a crystal grain size of the polycrystal silicon that comprises said channel area.

4. (Currently Amended) ~~The~~An insulated gate field effect transistor ~~according to claim 1~~having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity type source area thereof, wherein:

said channel area provides a single channel between said first and second conductivity type source areas and includes a non-overlapped area portion free from being overlapped by the gate electrode in plan, wherein:

said channel area is comprised of an intrinsic semiconductor.

5. (Previously Presented) The field effect transistor according to claim 4, wherein:

the non-overlapped area portion of said channel area contains injected impurities of less than 1 e−18/cm3.

6. – 9. (Cancelled)

10. (Currently Amended) ~~The~~An insulated gate field effect transistor ~~according to claim 9~~having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity type source area thereof, wherein:

said channel area provides a single channel between said first and second source areas and said gate electrode comprises two separate subgate electrodes disposed on respective sides of said first and second conductivity type source areas in a direction in which said channel area extends, wherein:

said channel area is comprised of an intrinsic semiconductor.

11. (Previously Presented) The field effect transistor according to claim 10, wherein:

the channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan and the area portion of said channel area contains injected impurities of less than 1 e−18/cm3.

12. (Previously Presented) A double field effect transistor device of an insulated gate type, comprising:

a channel area taking a virtually H-type form in plan;

a first pair of source areas different in conductivity type from one another respectively formed at opposite ends of one of a pair of parallel strips that comprises a part of the H, wherein a first single channel is provided in said channel area coupling between both of said first pair of source areas;

a second pair of source areas different in conductivity type from one another respectively formed at opposite ends of the other of said pair of parallel strips that comprises a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in conductivity type, wherein a second single channel is provided in said channel area coupling between both of said second pair of source areas; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that comprises a part of the H and a central link of the H that combines said pair of parallel strips.

13. (Previously Presented) The field effect transistor according to claim 12, wherein:

said channel area is comprised of an intrinsic semiconductor.

14. (Previously Presented) The field effect transistor according to claim 13, wherein:

the channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan and the area portion of said channel area contains injected impurities of less than 1 e−18/cm3.

15. (Previously Presented) An image display apparatus comprising a display unit of a plurality of pixels formed on an insulating substrate, and a controller formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein:

at least part of said controller is comprised of an insulated gate type field effect transistor having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity type source area thereof; and

said channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan.

16. (Previously Presented) An image display apparatus comprising a display unit of a plurality of pixels formed on an insulating substrate, and a controller formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein:

at least part of said controller is comprised of an insulated gate type field effect transistor having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity source area thereof; and

said channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan; and said apparatus comprising:

an image control unit of said display unit being of an insulated gate type, said image control unit comprising:

a channel area taking a virtually H-type form;

a first pair of source areas different in conductivity type from one another respectively formed at opposite ends of one of a pair of parallel strips that comprises a part of the H, wherein a first single channel is provided in said channel area coupling between both of said first pair of source areas;

a second pair of source areas different in conductivity type from one another respectively formed at opposite ends of the other of said pair of parallel strips that comprises a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in conductivity type, wherein a second single channel is provided in said channel area coupling between both of said second pair of source areas; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that comprises a part of the H and a central link of the H that combines said pair of parallel strips.

17. – 19. (Cancelled)

20. (Previously Presented) An insulated gate field effect transistor having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity type source area thereof, wherein:

said channel area comprises an area portion free from being overlapped by the gate electrode in plan,

wherein said channel area is comprised of a polycrystal silicon film, and

wherein the non-overlapped area portion of said channel area has a length longer than a crystal grain size of the polycrystal silicon that comprises said channel area.

21. (Previously Presented) An insulated gate type field effect transistor having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity type source area thereof, wherein:

said gate electrode comprises two separate subgate electrodes disposed on respective sides of said first and second conductivity type source areas in a direction in which said channel area extends, and

said channel area is comprised of an intrinsic semiconductor.

22. (Previously Presented) The field effect transistor according to claim 21, wherein:

the channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan and the area portion of said channel area contains injected impurities of less than 1 e−18/cm3.

23. (Previously Presented) A double field effect transistor device of an insulated gate type, comprising:

a channel area taking a virtually H-type form in plan;

a first pair of source areas different in conductivity type from one another respectively formed at opposite ends of one of a pair of parallel strips that comprises a part of the H;

a second pair of source areas different in conductivity type from one another respectively formed at opposite ends of the other of said pair of parallel strips that comprises a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in conductivity type; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that comprises a part of the H and a central link of the H that combines said pair of parallel strips.

24. (Previously Presented) The field effect transistor according to claim 23, wherein:

said channel area is comprised of an intrinsic semiconductor.

25. (Previously Presented) The field effect transistor according to claim 24, wherein:

the channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan and the area portion of said channel area contains injected impurities of less than 1 e−18/cm3.

26. (Previously Presented) An image display apparatus comprising a display unit of a plurality of pixels formed on an insulating substrate, and a controller

formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein:

at least part of said controller is comprised of an insulated gate type field effect transistor having a gate electrode overlapping a channel area between a first conductivity type source area and a second conductivity source area thereof; and

said channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan; and said apparatus comprising:

an image control unit of said display unit being of an insulated gate type, said image control unit comprising:

a channel area taking a virtually H-type form;

a first pair of source areas different in conductivity type from one another respectively formed at opposite ends of one of a pair of parallel strips that comprises a part of the H;

a second pair of source areas different in conductivity type from one another respectively formed at opposite ends of the other of said pair of parallel strips that comprises a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in conductivity type; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that comprises a part of the H and a central link of the H that combines said pair of parallel strips.